

**AN002E**

# **COMPLEX MEMORY INTERFACE IC'S**

## **SIMPLIFY MPU SYSTEM DESIGN**

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# THE SYSTEM

Today's sophisticated single-chip microcomputers (MCUs) are often presented as complete systems capable of achieving a variety of complex end functions. Such presentations habitually skirt the problems of "interface" — circuits required to match even the most elaborate MCU to a specific load. And what is true for MCUs is infinitely more true for microprocessors (MPUs), most of which make no pretense, whatever, at on-chip interface.

As microprocessor families mature, as in the case of a number of 8-bit NMOS MPUs today, more and more interface ICs — MSI and LSI parts — appear in the family offerings. Yet, since such components normally use NMOS technology, with its inherent voltage and current limitations, they are directed more toward data manipulation than to output drive capability. Thus, where significant output capability is required, the design of dedicated interface circuits normally falls to the system designer, using available bipolar SSI logic, often with a liberal sprinkling of discrete components.

The rapid expansion of microcomputers into applications requiring greater drive capability than available with standard NMOS components and the increasing need for high-speed control has spurred the development of bipolar integrated circuits specifically dedicated to providing the necessary interface. At Motorola, recent introductions by the linear IC department emphasize this trend.

Of special interest are four relatively new circuits, that form the more complex address and timing functions between

a typical 8-bit NMOS MPU and a large dynamic memory system. They are:

Dynamic Memory Controller - MC3480

Address Multiplexer/Refresh Counter, for 16-pin 16Kx1 dynamic memories - MC3242A

Address Multiplexer/Refresh Counter, for 16-pin 4Kx1 dynamic memories - MC3232A

Octal 3-States Buffer/Latch, for memory arrays using the new 64K memory packages - MC6882A/B

Actually only two of the above circuits are required to accomplish the complex addressing function, the specific lineup depending on the size of the memory device to be used — the 4K MCM4027, the 16K MCM4116, or the new 64K MCM6664.

Just how complex is this interface? The block diagram of Figure 1 helps tell the story. On the left portion of the diagram is an 8-bit MPU and its associated clock. All inputs and outputs of this MPU go to the microprocessor bus and, from there, to the circuits and peripherals controlled by the MPU — in this case, an external 64Kx8 dynamic memory array on the right portion of the diagram.

Ideally, we'd like to connect the memory array directly to the other end of the bus so that direct communications between the two portions of the system could occur. But there are problems.

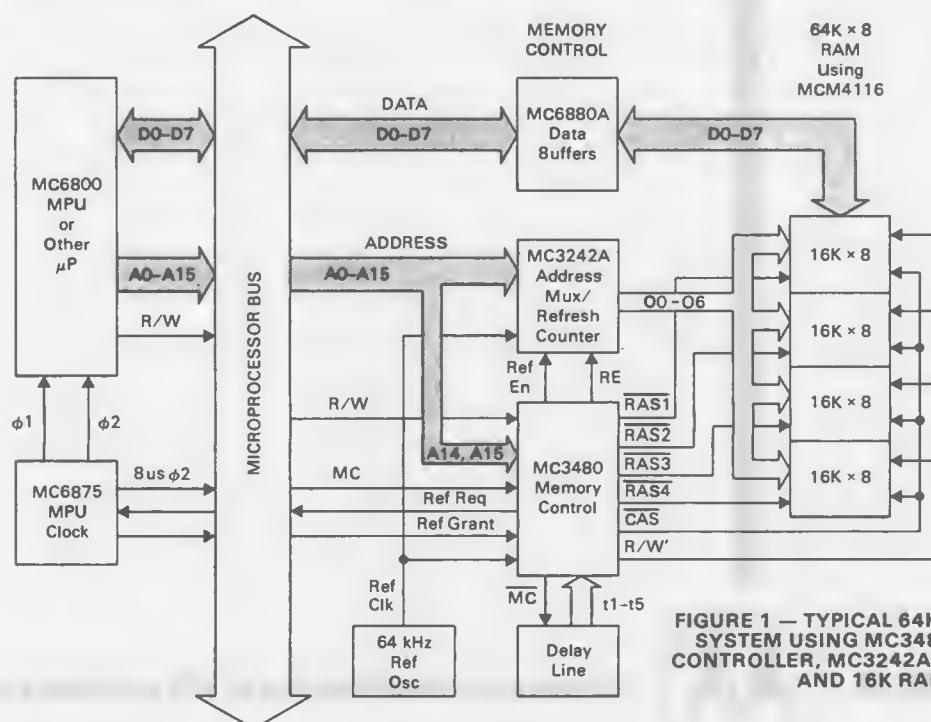


FIGURE 1 — TYPICAL 64K x 8 MEMORY SYSTEM USING MC3480 MEMORY CONTROLLER, MC3242A MULTIPLEXER AND 16K RAM.

## Data Bus Buffering

Starting with the simplest one we see, at the top of the diagram, that the 8-bits of data (D0-D7) linking the MPU to the memory array must first be buffered.

Why ?

Because the data output from the MPU is sufficient to drive only a half-dozen or so external circuits. Certainly not the 32 separate 16Kx1 memory packages, that must be hung on the end of the data bus to constitute a 64K byte array, not to mention any other peripheral circuits that must be addressed.

Enter, the MC6880A Data Buffers.

The 6880A is a bus transceiver that lets data travel in both directions between the MPU and the load. It has a high input impedance so that it doesn't load down the source, and enough output current (48 mA driver and 20 mA receiver output) to handle even the more complex MPU loads comfortably.

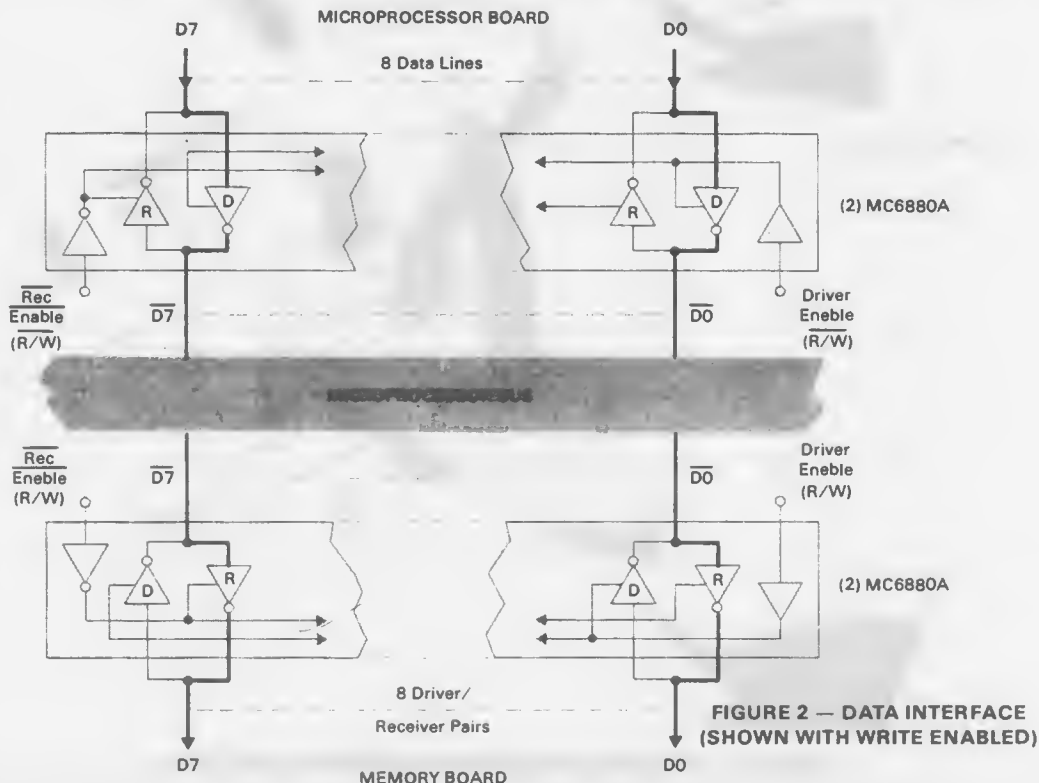
The device is not new and, actually, it's even a bit outdated. It has only four external driver-receiver pairs, whereas the MPU data bus requires eight. This means that a functional system typically requires four individual packages (Figure 2) to accomplish this rather simple buffering functions. But it's the best that the industry has to offer at this time, and it emphasizes the proliferation of interface circuits in a functional system. Obviously, there is an urgent need of greater density in interface packaging.

## Address Bus Interface

The interface requirements of the data bus are multiplied many times by the demands made by a large dynamic memory system on the address and control bus. These not only need the same degree of buffering as the data bus, but additional circuitry within their paths must provide :

1. Address Decoding — the ability to select one specific 16Kx8 sub-block from among the 4 blocks in a 64Kx8 system (using the 16 Kx1 memory packages).
2. Memory Refresh — the capability of periodically addressing each memory row and replenishing any charge that may have leaked off the individual memory cells.
3. Memory Multiplexing — the ability to divide a full 16-bit address-bus signal into two components that are applied, sequentially, as row-address and column-signals to the memory, with the proper timing and control signals.

The last function applies specifically and exclusively to the popular 16-pin memories that use address multiplexing as a means for reducing the number of pins required to access the chip. Obviously, each interface function is uniquely related to specific load (type of memory array) so that the interface circuitry can not be an integral portion of the MPU. Recently the demand for such circuits has become large enough to permit cost-effective production as standard, off-the-shelf integrated circuits. The address-interface circuits discussed here are examples of this trend.



## Circuit Requirements

Address multiplexing came about as the most productive means for increasing board density and reducing manufacturing cost of large memory arrays. It's implementation reduces the number of address input pins by as many as eight for a 64K RAM (a reduction of six pins for a 4K RAM), thus permitting the use of a 16-pin package rather than the 22 (or more) pins previously required. Of course, one pays for this savings thru the need for multiplex control, but that is considered a low price compared with the resulting benefits.

To address a 64K byte array composed of 16K-bit memory package, the 16-bit address bus may be considered to be divided into three parts, Figure 3. The least significant seven bits (A0-A6) are the row-address bits, to select one of 128 different rows. The next seven (A7-A13) are assigned to address the 128 different columns. The most significant two bits (A14 and A15) select the desired 1-of-4 different memory blocks that make up the array.

Multiplexing is achieved with two signals — a Row-Address-Strobe (RAS) and a Column-Address-Strobe ( $\overline{\text{CAS}}$ ) signal which, sequentially (rather than

simultaneously), strobe the row and column addresses into the individual memories. By using the address input pins of the memory first for the row bits and then for the column bits of the total address, the required number of input pins cut is in half. The problem becomes one of generating the timing sequence for the control signals so that :

1. the row-and column-address bits are applied, sequentially, to the address inputs of the memory;
2. the  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  signals are applied in conjunction with the row- and column-address bits, respectively

that, in addition to the normal requirements for dynamic memory control — refresh timing, Read/Write selection, and signal buffering.

Tracing the operations of the required interface functions through the circuitry not only provides an appreciation for the design time that is saved by the availability of such dedicated functions, but also of the complexity of such functions which are often totally ignored in discussion of MPU/MCU applications.

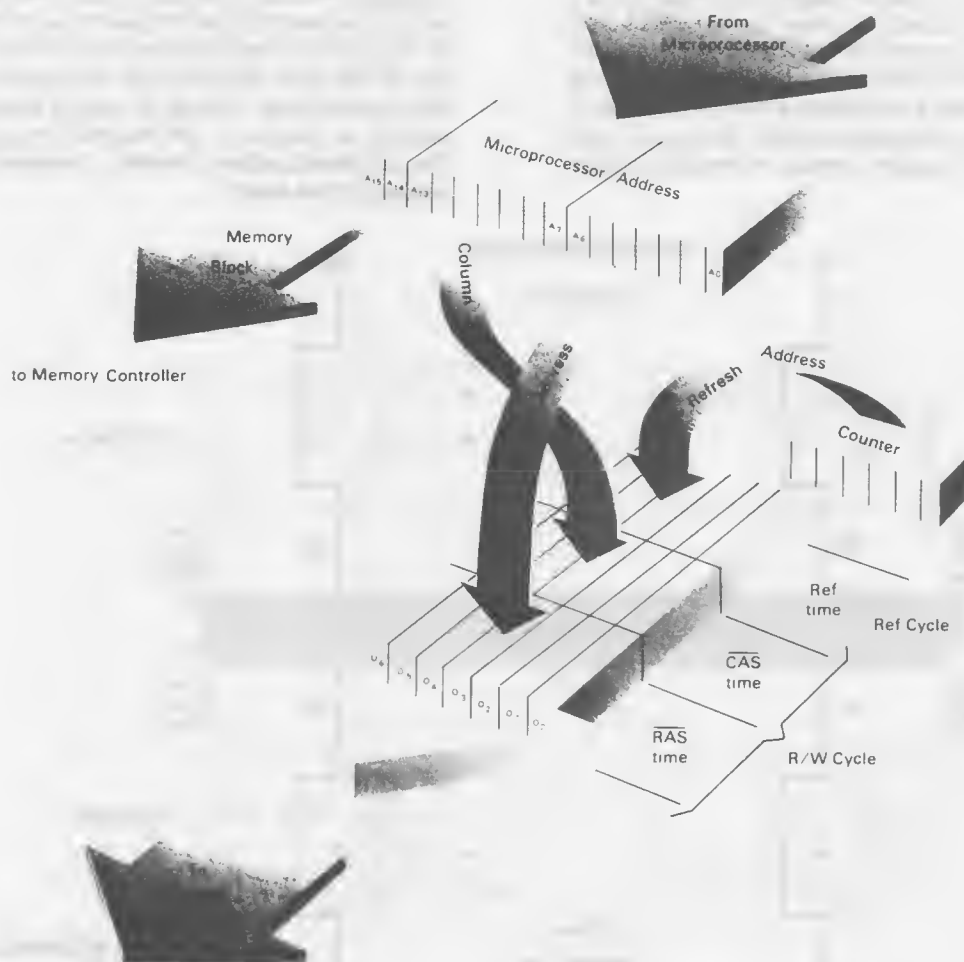


FIGURE 3 — ROW/COLUMN/REFRESH ADDRESS MULTIPLEXING

## Addressing the Memory Array

In operation, actual memory addressing is accomplished through the multiplexing capability of the Address Multiplexer and Refresh counter circuit, MC3424A (or MC3232A, depending on the size of memory array), while the timing, refresh control, and high order decode is provided by the MC3480 Memory Controller. Examining first the Address Multiplexer, its sole function is to guarantee that when the Controller generates a  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  or Refresh signal, the corresponding address actually appears on the output of the Multiplexer for application to the Address lines of the memory. The operation can be followed with the aid of Figure 4.

The Multiplexer contains seven individual gate arrays\*, each comprising three AND gates driving a single NOR gate. Each of the AND gates of an array is associated with one of the three addresses that must be applied to the memory. When the Row Enable input of the circuits is "high" and Ref En is low, all the Row-Address gates are

\* Seven bits are required to address the 128 rows and columns of a 16K memory. A 4K memory would require only a 6-bit address for its 64 rows and columns.

turned on (at the same time, the Column-Address gates are turned off), and the output of the multiplexer reflects the states of the first 7 address-input bits (A0-A6). When the Row Enable input goes low (Ref En still low), the Column-Address gates are turned on (the Row-Address gates are turned off), and the multiplexer output now reflects the state of the column-address input bits (A7-A13).

When a refresh is required, once every 2 milliseconds for each row of memory locations, the Refresh Enable input is brought "high" in response to a signal from the 64 kHz (clock) oscillator. The Refresh AND gates are activated and the multiplexed outputs now reflect the content of the 7-bit counter. This is the refresh address, which is applied to the memory coincident with a  $\overline{\text{RAS}}$  signal. At the trailing edge of the clock signal the 7-bit counter is incremented so that, during the next Refresh cycle, the next memory row in each of the four memory blocks will be addressed for refreshing. Since there are 128 rows to be addressed in 0.002 second, the clock frequency must be:

$$\frac{1}{0.002} \times 128 = 64,000 \text{ Hz}$$

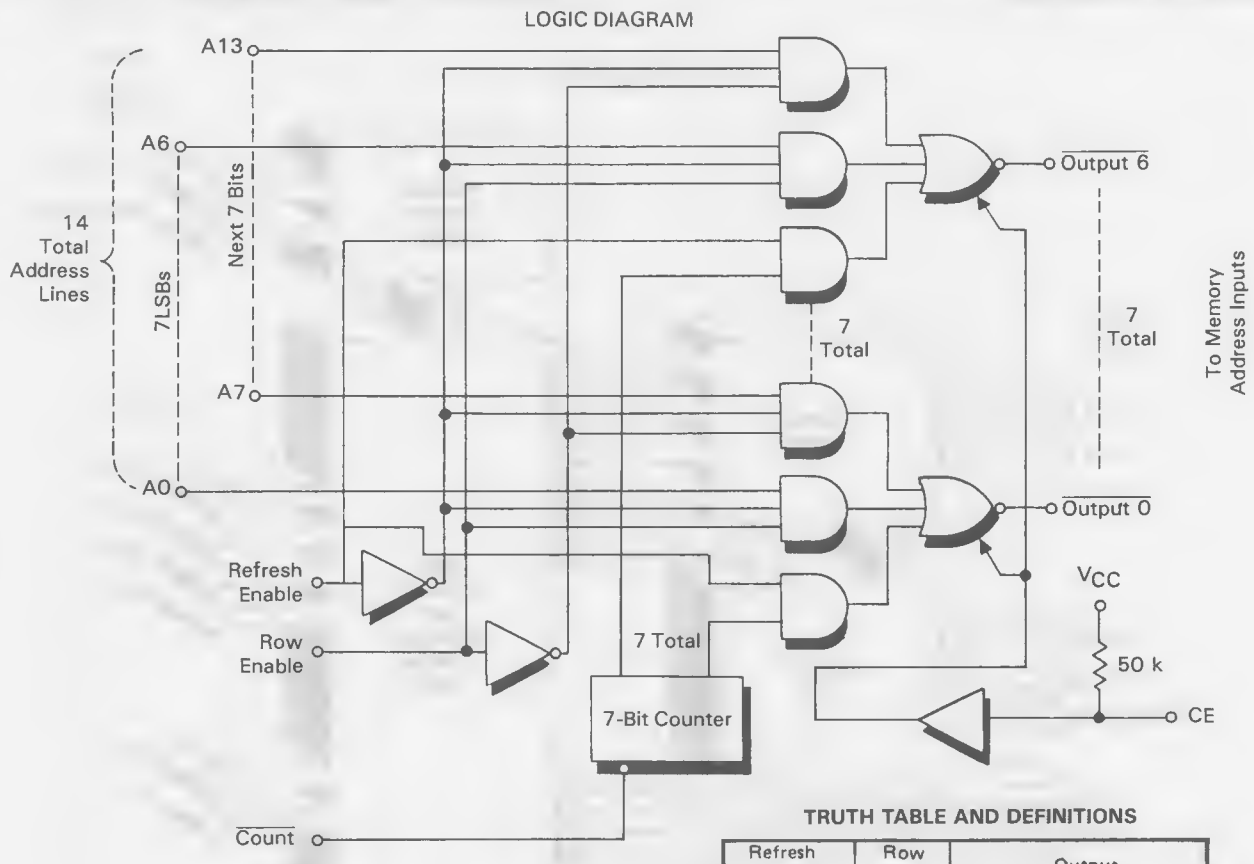


FIGURE 4 — MC3424A LOGIC DIAGRAM

## The memory Controller

All memory timing signals originate, of course, with the MPU clock and the Refresh clock, but the apportionment of these to the right place at the right time is the function of a rather complex controller — MC3480.

The block diagram of Figure 5 shows a myriad of inputs and outputs and permits an analysis of the functions.

For example:

When the MPU puts out an address over the 16-bit address bus, the fourteen low-order addresses are multiplexed to generate the row and column address of the four 16Kx8 memory arrays shown in Figure 1. It remains for the two high-order bits (A14 and A15) of the address to select the specific 1-of-4 memory blocks to be activated. These two high-order bits are applied to the controller decoded, and outputted as a  $\overline{RAS1}$ ,  $\overline{RAS2}$ ,  $\overline{RAS3}$  or  $\overline{RAS4}$  signal to select the specific block that houses the desired address. The remaining three blocks, though they are addressed simultaneously by the output of the multiplexer, remain unselected because their  $\overline{RAS}$  inputs remain unactivated.

Now an interesting interaction occurs between the memory controller and the multiplexer. Although the address from the MPU is appropriately applied to the controller and multiplexer, it is not yet determined whether the output of the multiplexer is a Row address (bits 0-6), or a Column address (bits 7-13). To achieve this, the controller sends a Row Enable signal to the multiplexer. As can be determined from Figure 3, when this signal is "high", the multiplexer output is the Row address. When the signal goes "low", the Column address is outputted. Thus, with proper timing, the Row address is strobed into the memory first, followed by the Column address.

To understand the sequence of events in a typical memory read or write cycle, let us trace through the timing diagram of Figure 6.

It all starts in the Master Clock generator that is either an integral part of the MPU, or a closely associated separate circuit. The MC generates the basic frequency that starts each successive memory address cycle. It also generates (normally) a signal that is twice the fundamental frequency ( $f_0$ ), and one that is 4 times  $f_0$ . These various signals are applied to the t1 through t5 inputs of the memory controller where they start a closely coordinated timing sequence that governs the operation of the memory system. The operation is as follows:

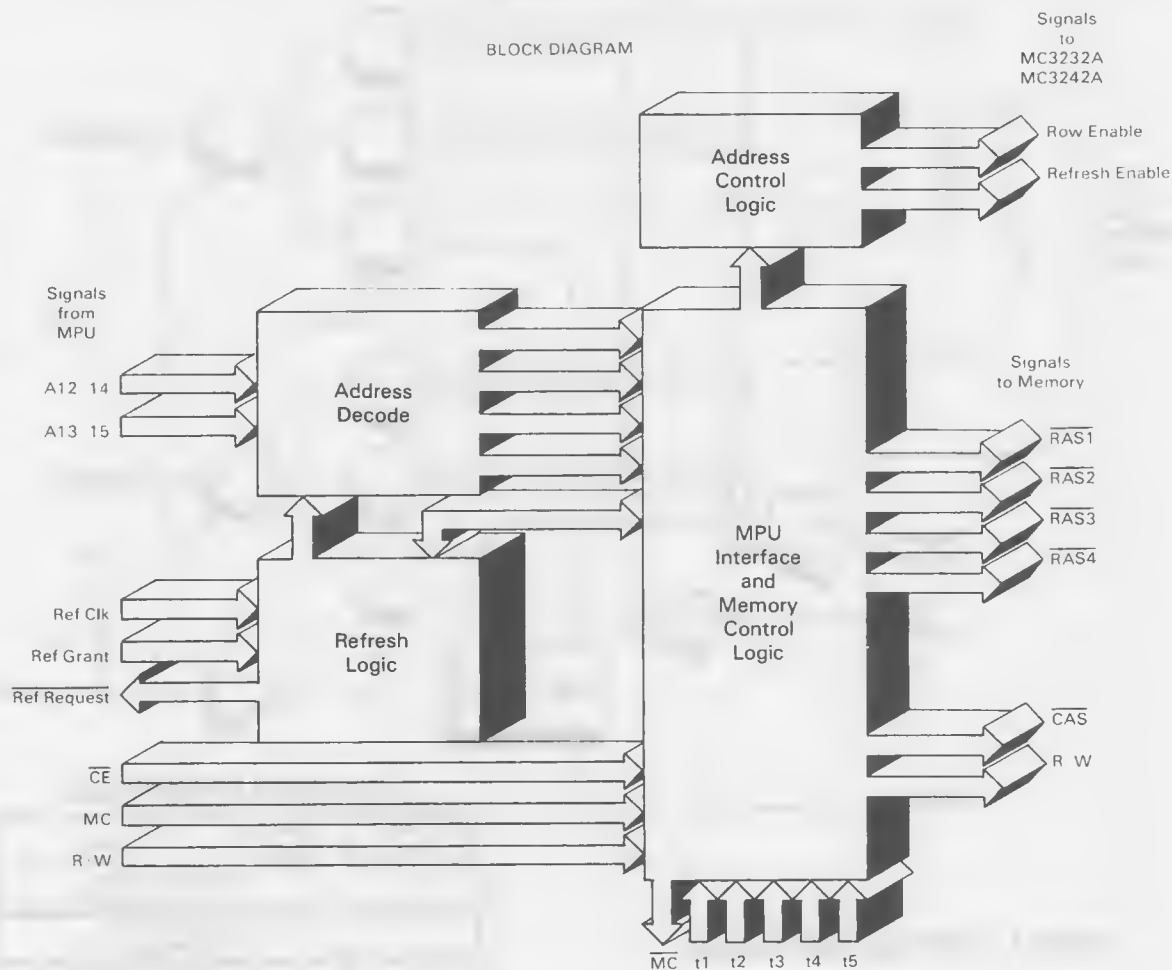


FIGURE 5 — MC3480 MEMORY CONTROLLER

1. At time  $t_0$  the Master Clock of the system goes negative beginning the cycle.
2. Sometime between  $t_0$  and  $t_1$ , the MPU places the memory address on the Address Bus and, consequently, to the inputs of the Multiplexer (bits A0-A13) and Controller (bits A14 and A15). At that point, the Row Enable output applied by the Controller to the Multiplexer is "high", and the Multiplex output (00-06) represents the Row Address, A0-A6.
3. At  $t_1$ , a positive signal applied to the  $t_1$  input of the Controller sends a  $\overline{\text{RAS}}$  output to the 1-of-4 memory array selected by bits A14 and A15, strobing the Row Address into the memory latches.
4. An instant later, in response to a  $t_2$  signal (from  $4f_0$ ) a negative-going Row Enable signal from the Controller to the Multiplexer causes the Multiplex output to change to the column address (bits A7-A13), and...

5. ... at  $t_3$  the  $\overline{\text{CAS}}$  circuit within the Controller goes low, strobing the column address bits into the memory.
6. At  $t_4$ , the Controller responds to a Read/Write input from the MPU and drives the memory R/W line low at the proper time if a Write cycle has been selected by the MPU R/W line.
7.  $t_5$  ends the memory address cycle by resetting all the associated outputs to a "high" level until the entire sequence is initiated again by the next transition of the Master Clock.

The use of basic clock signals such as  $2xf_0$  and  $4xf_0$  to trigger controller outputs when these clock signals change state more than once per memory cycle is made possible by another feature of the MC3480. The  $t$  inputs are daisy-chained to make them easy to use. Once an output has occurred during a memory cycle, it cannot reoccur even though its  $t$  input is changed.

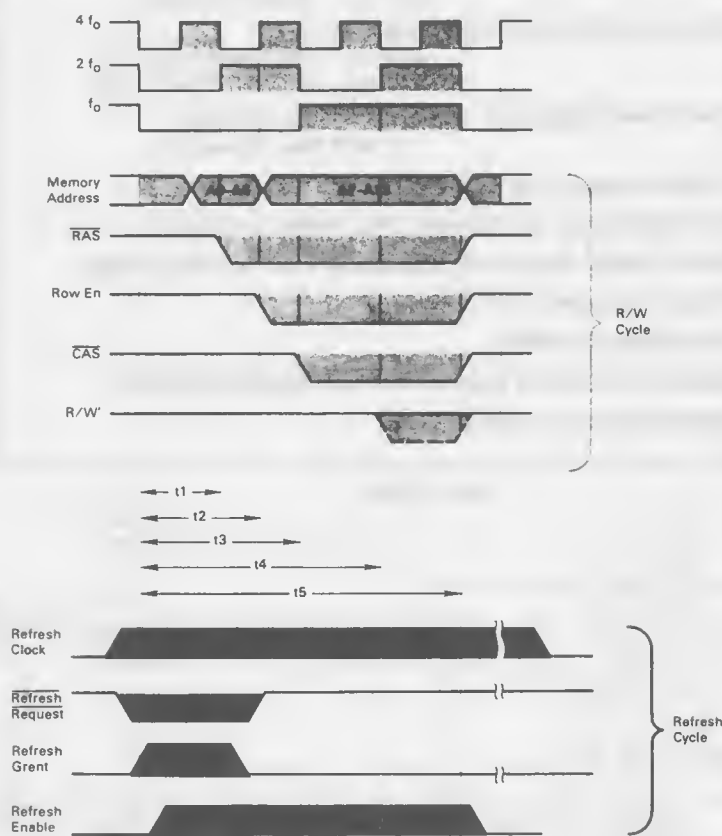


FIGURE 6. TIMING DIAGRAM

For a Refresh sequence, the cycle is initiated by a positive transition of the Refresh Clock, in response to which the Controller sends a Refresh Request signal to the MPU. The MPU finishes its present operation and then sends back a Refresh Grant signal. This immediately triggers the Refresh Enable signal which, when applied to the Multiplexer, turns off the Row and Column AND gates and turns on the Ref AND gates placing a Refresh address on the memory Address Bus; After 128 Refresh cycles, the entire array will have been refreshed.

The above description, though simplified, clearly indicates the considerable amount of logic required to perform the Controller function. In fact, if the interface function served by the two components described were to be implemented with SSI functions of the TTL variety, upward of a dozen individual logic packages would be needed. Clearly, the interface requirement represents a significant portion of a microcomputer design effort and component complement, a requirement that is being considerably simplified as Interface goes LSI.

**Editor's Note:** The MC3480/MC3242A component complement described is used for a 64Kx8 byte memory array utilizing MCM4116B (16K) memory packages:

For a 16K memory utilizing the MCM4027A (4K) memory packages, the MC3480/MC3232A component complement would be employed in an identical manner.

The new MCM6664 (64K) dynamic RAMs have a built-in refresh counter. They, therefore, require only the MC3480 Memory Controller in conjunction with the latch (multiplex) function provided by the newly-introduced MC6882B Octal Buffer Latch.

# THE MEMORIES

## MCM4027A

### 4096-BIT DYNAMIC RANDOM ACCESS MEMORY

#### 4096-BIT DYNAMIC RANDOM ACCESS MEMORY

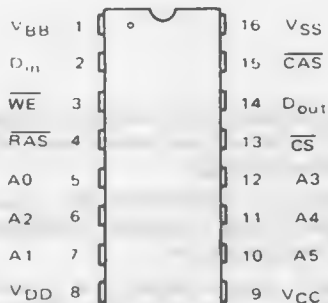
The MCM4027A is a 4096 x 1 bit high-speed dynamic Random Access Memory. It has smaller die size than the MCM4027 providing improved speed selections. The MCM4027A is fabricated using Motorola's highly reliable N-channel silicon-gate technology.

By multiplexing row and column address inputs, the MCM4027A requires only six address lines and permits packaging in Motorola's standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated.

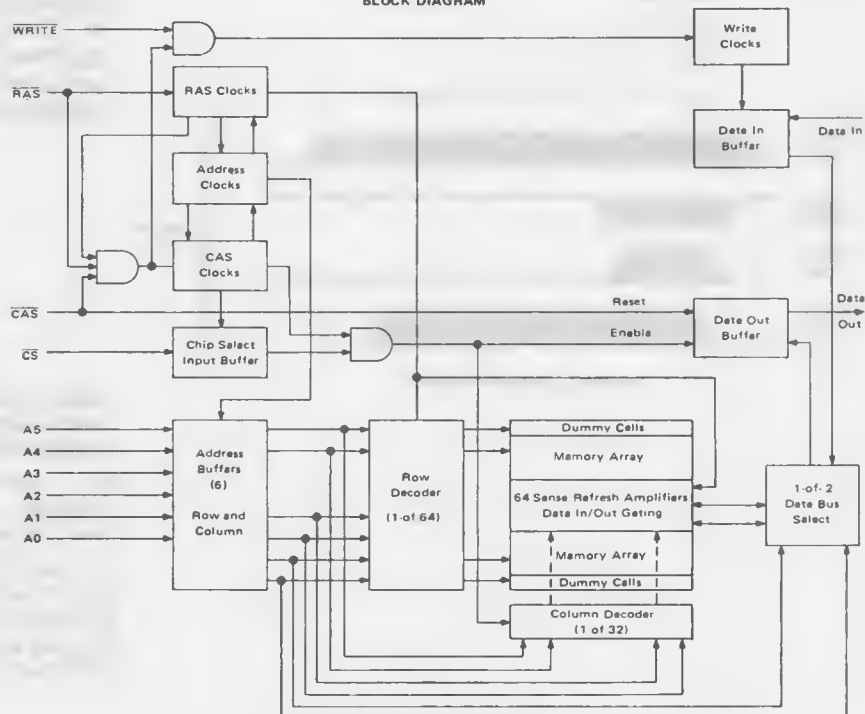
All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM4027A incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64 row addresses requiring a refresh cycle every 2.0 milliseconds.

- Maximum Access Time = 120 ns — MCM4027AC1  
150 ns — MCM4027AC2  
200 ns — MCM4027AC3  
250 ns — MCM4027AC4
- Maximum Read and Write Cycle Time =  
320 ns — MCM4027AC1, C2  
375 ns — MCM4027AC3, C4
- Low Power Dissipation — 470 mW Max (Active)  
27 mW Max (Standby)
- 3-State Output for OR-Ties
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Industry Standard 16-Pin Package
- Page-Mode Capability
- Compatible with the Popular 2104/MK4096/MCM6604
- Second Source for MK4027

#### PIN ASSIGNMENT



#### BLOCK DIAGRAM

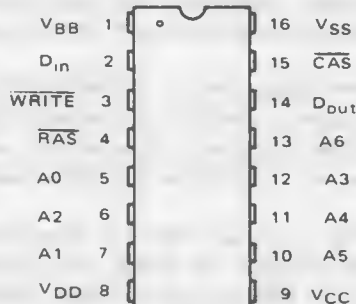




# MCM4116B

## 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

### PIN ASSIGNMENT



### PIN NAMES

A0-A6	Address Inputs
CAS	Column Address Strobe
D <sub>in</sub>	Data In
D <sub>out</sub>	Data Out
RAS	Row Address Strobe
WRITE	Read/Write Input
VBB	Power (-5 V)
VCC	Power (+5 V)
VDD	Power (+12 V)
VSS	Ground

## 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116B is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

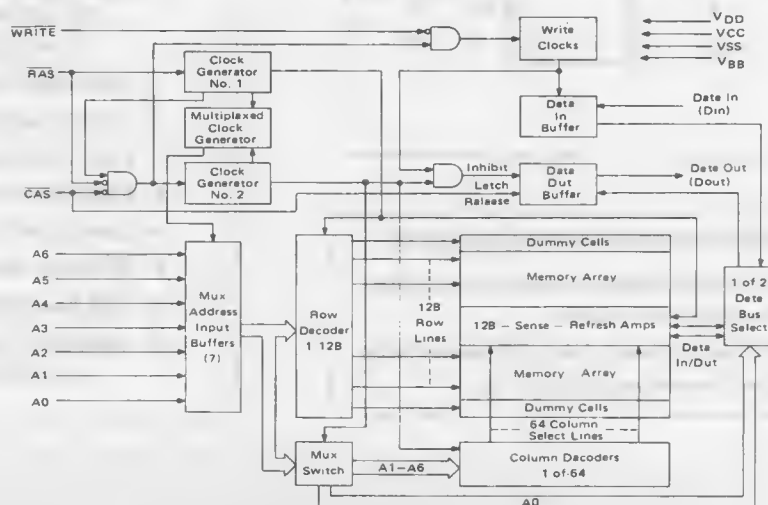
By multiplexing row and column address inputs, the MCM4116B requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116B is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

The MCM4116B incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- $\pm 10\%$  Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation — 426 mW Active, 20 mW Standby (Max)
- Fast Access Time Options: 150 ns — MCM4116BP-15, BC-15  
200 ns — MCM4116BP-20, BC-20  
250 ns — MCM4116BP-25, BC-25  
300 ns — MCM4116BP-30, BC-30
- Easy Upgrade from 16-Pin 4K RAMs

### BLOCK DIAGRAM



# MCM4516

## 16,384-BIT DYNAMIC RAM

### PIN ASSIGNMENT

REFRESH	1	16	V <sub>SS</sub>
D	2	15	$\overline{\text{CAS}}$
$\overline{\text{W}}$	3	14	Q
$\overline{\text{RAS}}$	4	13	A <sub>6</sub>
A <sub>0</sub>	5	12	A <sub>3</sub>
A <sub>2</sub>	6	11	A <sub>4</sub>
A <sub>1</sub>	7	10	A <sub>5</sub>
V <sub>CC</sub>	8	9	N/C

### ON-CHIP REFRESH FEATURES/BENEFITS

Reduce System Refresh Controller Design Problem  
 Reduce System Parts Count  
 Reduce System Noise Increasing System Reliability  
 Reduce System Power During Refresh

## 16,384-BIT DYNAMIC RAM

The MCM4516 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high-performance, N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM4516 requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by  $\overline{\text{CAS}}$  allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM4516 incorporates a one-transistor cell design and dynamic storage techniques. In addition to the  $\overline{\text{RAS}}$ -only refresh mode, refresh control function available on pin 1 provides automatic and self-refresh modes.

- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 120 ns Operation
- Low Power Dissipation:
  - 200 mW Maximum (Active)
  - 20 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Output Capability
- 64K Compatible 128-Cycle, 2 ms Refresh
- Control on Pin 1 for Automatic and Self Refresh
- $\overline{\text{RAS}}$ -only Refresh Mode
- $\overline{\text{CAS}}$  Controlled Output Providing Latched or Unlatched Data
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K RAM (MCM6664)

# MCM4517

16,384-BIT  
DYNAMIC RAM

**PIN ASSIGNMENT**

N/C	1	16	VSS
D	2	15	$\overline{\text{CAS}}$
$\overline{\text{W}}$	3	14	Q
$\overline{\text{RAS}}$	4	13	A6
A0	5	12	A3
A2	6	11	A4
A1	7	10	A5
VCC	8	9	N/C

## 16,384-BIT DYNAMIC RAM

The MCM4517 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high-performance, N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM4517 requires only seven address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by  $\overline{\text{CAS}}$  allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM4517 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 100 ns Operation
- Low Power Dissipation:
  - 150 mW Maximum (Active)
  - 14 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Output Capability
- 64K Compatible 128-cycle, 2 ms Refresh
- $\overline{\text{RAS}}$ -only Refresh Mode
- $\overline{\text{CAS}}$  Controlled Output
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K RAM (MCM6664)
- Allows Negative Overshoot  $V_{IL}$  Min = -2 V
- Hidden  $\overline{\text{RAS}}$  Only Refresh Capability

**32,768-BIT  
DYNAMIC RAM**

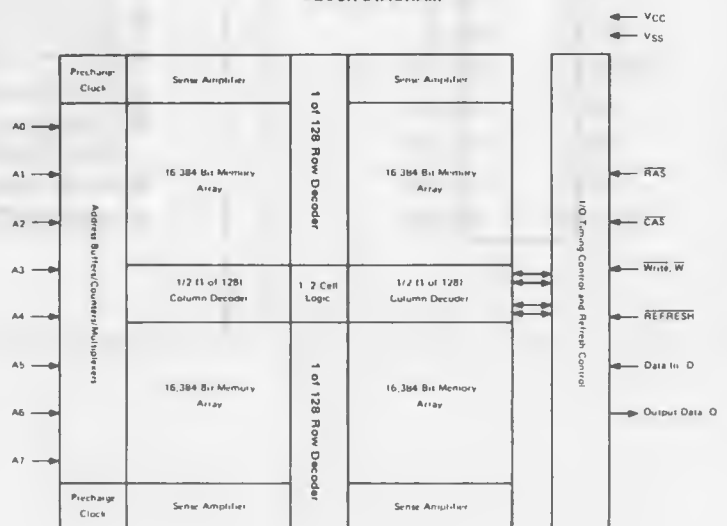
The MCM6633 is a 32,768 bit, high-speed, dynamic Random-Access Memory. Organized as 32,768 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6633 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 32,768 Words of 1 Bit
- Single +5 V Operation
- Fast 150 ns Operation
- Low Power Dissipation
  - 275 mW Maximum (Active)
  - 30 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Output Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- RAS-only Refresh Mode
- CAS Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4516, MCM4517)
- One Half of the 64K RAM MCM6665
- The Operating Half of the MCM6633 is Indicated by Device Marking:
  - MCM66330 Tie A7 CAS (A15) Low "0"
  - MCM66331 Tie A7 CAS (A15) High "1"

N/C*	1	16	V <sub>SS</sub>
D	2	15	$\overline{\text{CAS}}$
$\overline{\text{W}}$	3	14	Q
$\overline{\text{RAS}}$	4	13	A6
A0	5	12	A3
A2	6	11	A4
A1	7	10	A5
V <sub>CC</sub>	8	9	A7

### BLOCK DIAGRAM



# MCM6664

## 65,536-BIT DYNAMIC RAM

### 65,536-BIT DYNAMIC RAM

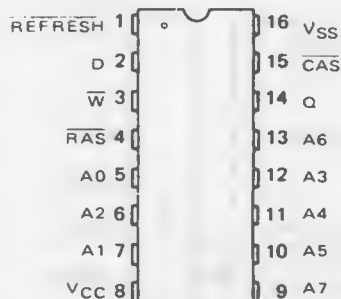
The MCM6664 is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6664 requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by  $\overline{\text{CAS}}$  allowing for greater system flexibility.

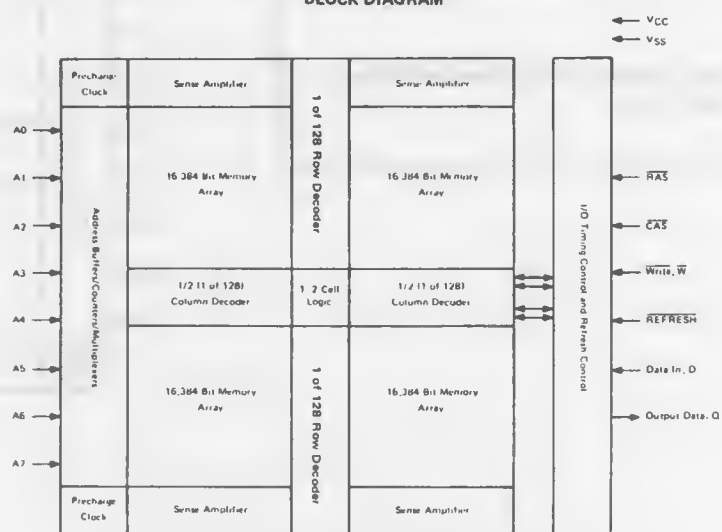
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6664 incorporates a one-transistor cell design and dynamic storage techniques. In addition to the  $\overline{\text{RAS}}$ -only refresh mode, refresh control function available on pin 1 provides automatic and self-refresh modes.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation
- Fast 150 ns Operation
- Low Power Dissipation
  - 275 mW Maximum (Active)
  - 30 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Output Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- Control on Pin 1 for Automatic and Self Refresh
- $\overline{\text{RAS}}$ -only Refresh Mode
- $\overline{\text{CAS}}$  Controlled Output Providing Latched or Unlatched Data
- Upward Pin Compatible from the 16K RAM (MCM4116)

### PIN ASSIGNMENT



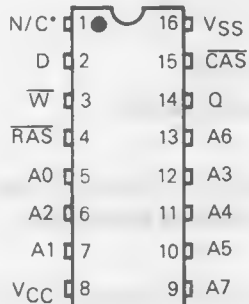
### BLOCK DIAGRAM



# MCM6665

## 65,536-BIT DYNAMIC RAM

### PIN ASSIGNMENT



\* internal pullup resistor should be left open or tied to V<sub>CC</sub>.

### 65,536-BIT DYNAMIC RAM

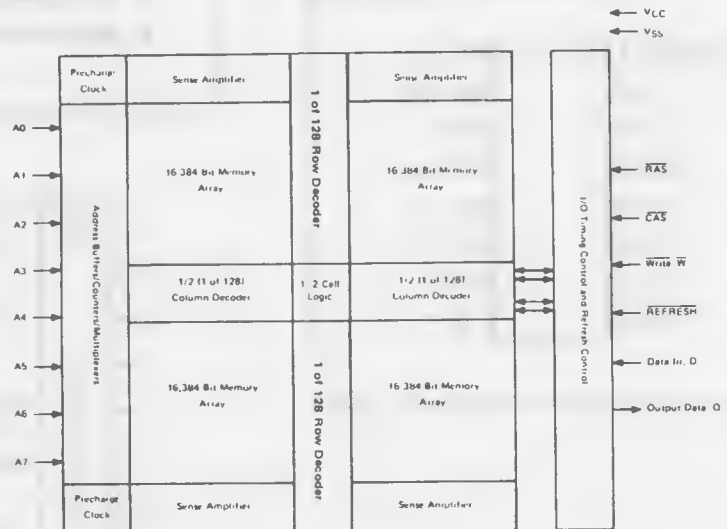
The MCM6665 is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6665 requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by  $\overline{CAS}$  allowing for greater system flexibility.

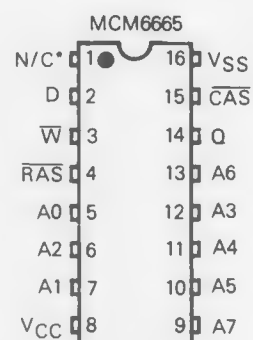
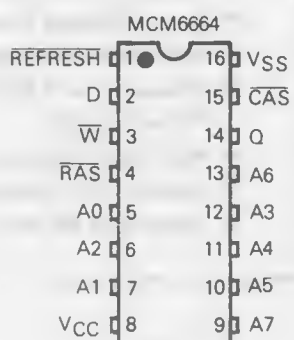
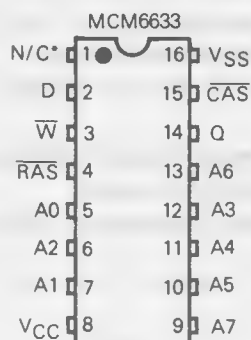
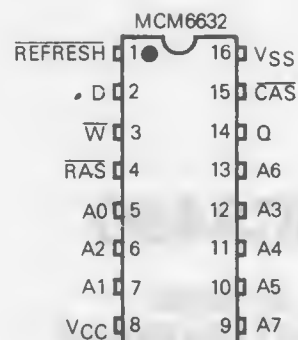
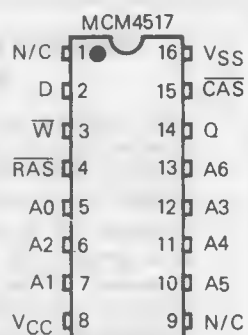
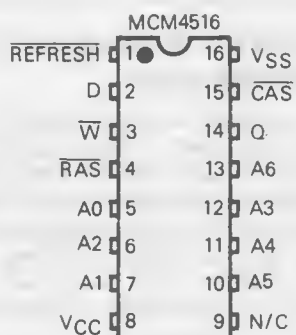
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation
- Fast 150 ns Operation
- Low Power Dissipation
  - 275 mW Maximum (Active)
  - 30 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$ -only Refresh Mode
- $\overline{CAS}$  Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)

### BLOCK DIAGRAM



## PIN ASSIGNMENT COMPARISON



### PIN VARIATIONS

Pin Number	MCM4116	MCM4516	MCM4517	MCM6632	MCM6663	MCM6664	MCM6665
1	$V_{BB}(-5\text{ V})$	REFRESH	N/C	REFRESH	N/C*	REFRESH	N/C*
8	$V_{DD}(+12\text{ V})$	VCC	VCC	VCC	VCC	VCC	VCC
9	$V_{CC}(+5\text{ V})$	N/C	N/C	A7	A7	A7	A7

\* internal pullup resistor should be left open or tied to VCC.

# THE SYSTEM CONTROLLER

## MC3480

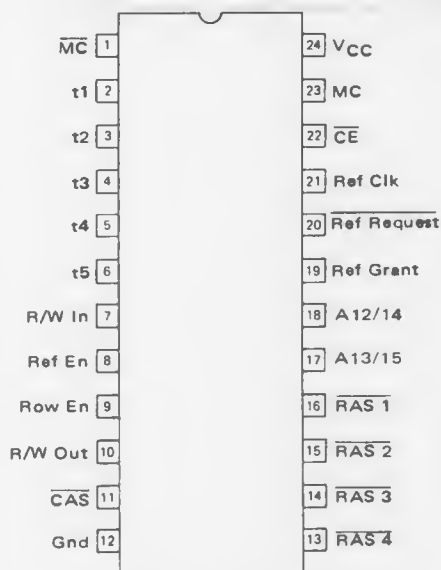
### DYNAMIC MEMORY CONTROLLER

#### MEMORY CONTROLLER FOR 16 PIN 4K, 16K AND 64K DYNAMIC RAMs

The memory controller chip is designed to greatly simplify the interface logic required to control the popular 16 pin multiplexed dynamic NMOS RAMs in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

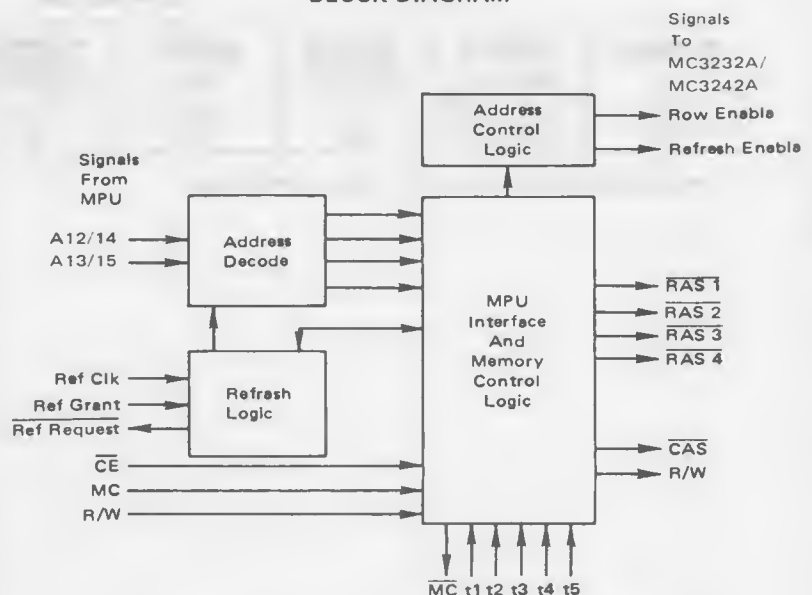
- Greatly Simplify the MPU-Dynamic Memory Interface
- Reduce Package Count and System Access/Cycle Times 30%
- Chip Enable for Expansion to Larger Word Capacity
- Generate 1 of 4 RAS Signals for an Optimum 16K/64K Memory System
- High Input Impedance for Minimum Loading of MPU Bus
- Schottky TTL Technology for High Performance
- Useful with 4K and 16K and Future Expanded Dynamic RAMs

#### PIN CONNECTIONS



See Pin Descriptions

#### BLOCK DIAGRAM



Several methods may be employed to generate the required time delay:

1. One shots
2. High frequency counters
3. High frequency shift registers
4. Delay lines
5. Signals from MPU Clock



# THE ADDRESS MULTIPLEXER REFRESH COUNTERS

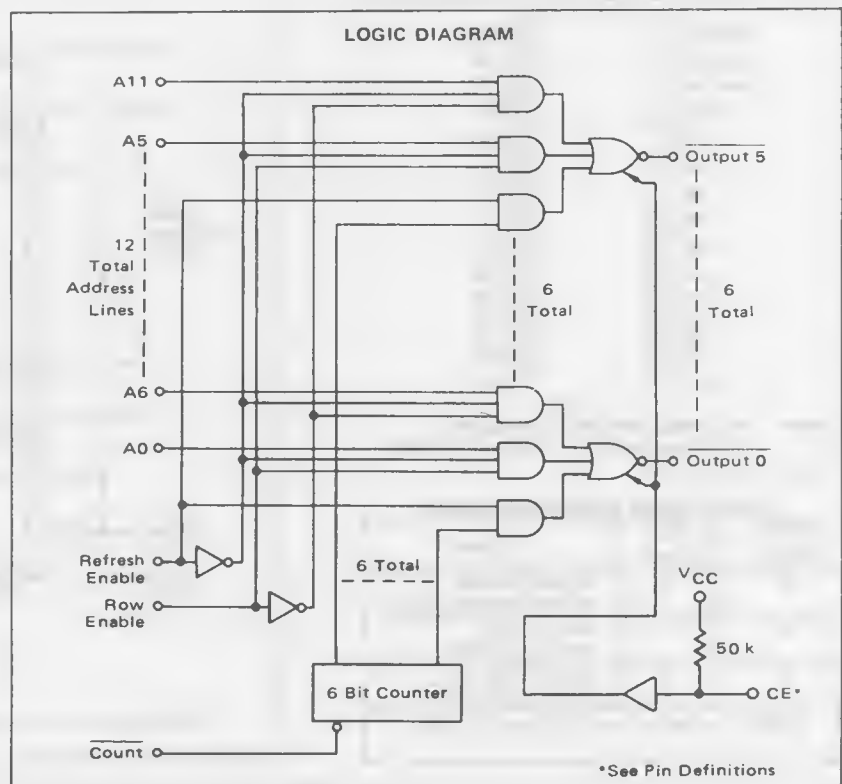
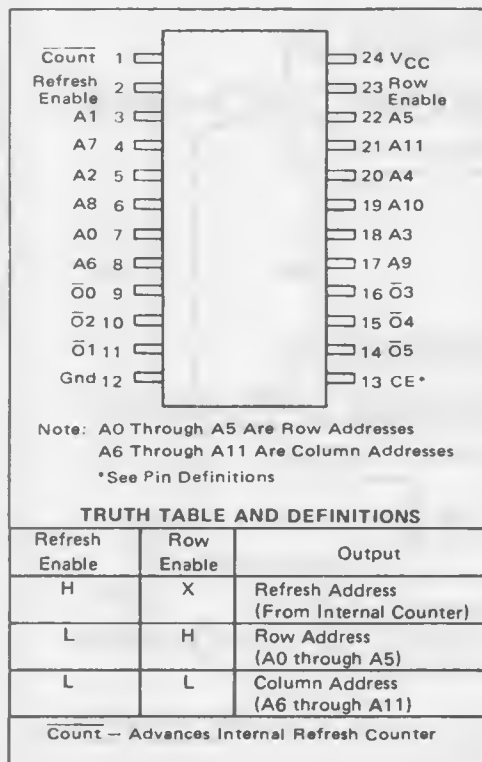
## MC3232A

### MEMORY MULTIPLEXER AND REFRESH ADDRESS COUNTER

#### MEMORY ADDRESS MULTIPLEXER

The Motorola MC3232A is an address multiplexer and refresh counter for 16-pin 4K dynamic RAMs that require a 64-cycle refresh. It multiplexes twelve system address bits to the six input address pins of the memory device. The MC3232A also contains a 6-bit refresh counter that is clocked externally to generate the 64 sequential addresses required for refresh. The high performance of the MC3232A will enhance the high speed of the fast N-channel RAMs such as the MCM4027.

- Simplifies 16-Pin 4K Dynamic Memory Design
- Reduces Package Count
- 6-Bit Binary Counter for 64 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus:
  - $I_F = 0.25 \text{ mA Max}$
- Schottky TTL for High Performance Address
  - Input to Output Delay
  - $t_{AO} = 25 \text{ ns @ } C_L = 250 \text{ pF}, 9.0 \text{ ns Max @ } C_L = 15 \text{ pF}$
- Second Source to Intel 3232
  - (Detect Zero Function Not Included and Additional Power Fail Feature Added at Pin 13)



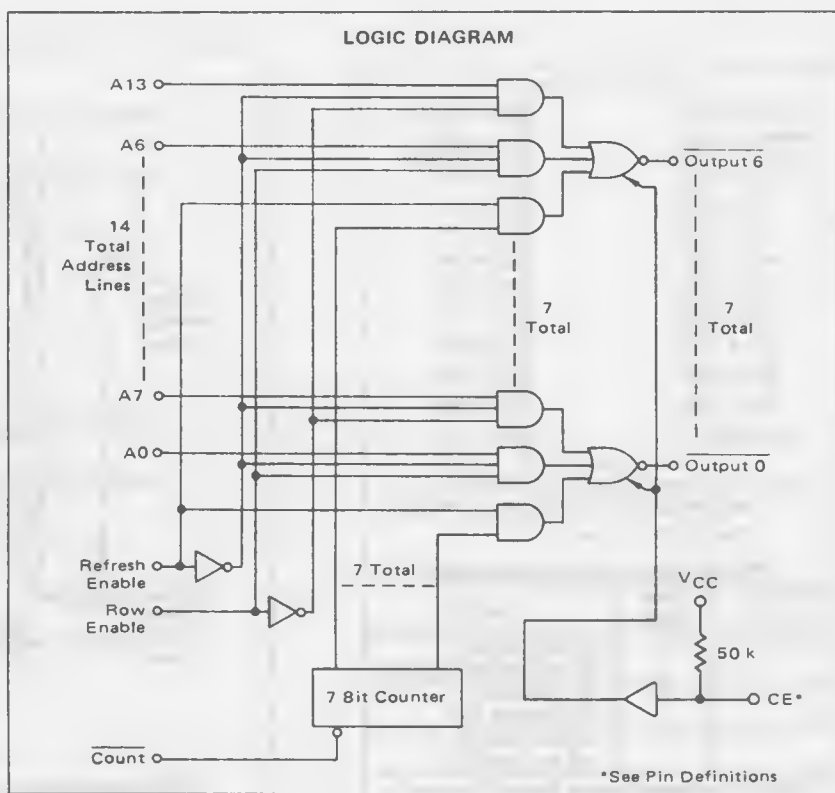
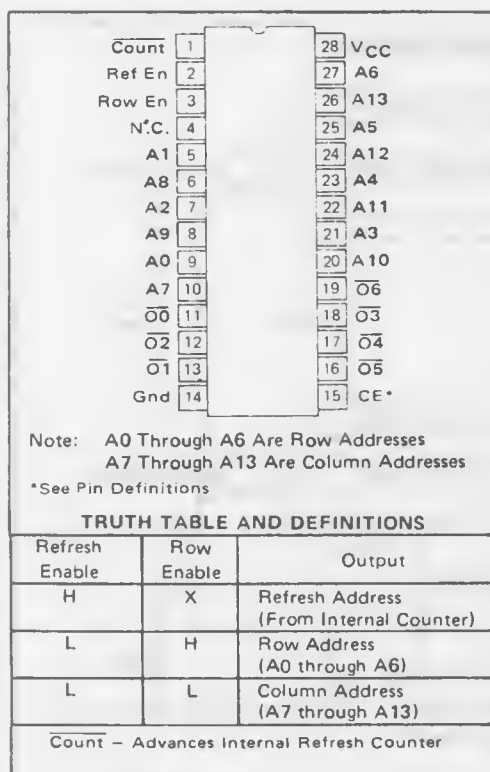
# MC3242A

## MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

### MEMORY ADDRESS MULTIPLEXER FOR 16K RAMS

The Motorola MC3242A is an address multiplexer and refresh counter for 16-pin 16K dynamic RAMs that require a 128-cycle refresh. It multiplexes fourteen system address bits to the seven address pins of the memory device. The MC3242A also contains a 7-bit refresh counter that is clocked externally to generate the 128 sequential addresses required for refresh. The high performance of the MC3242A will enhance the high speed of the N-channel RAMs such as the MCM4116.

- Simplifies 16-Pin 16K Dynamic Memory Design
- Reduces Package Count
- 7-Bit Binary Counter for 128 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus:  
 $I_F = 0.25 \text{ mA Max}$
- Schottky TTL for High Performance Address Input to Output Delay —  
 $t_{AO} = 25 \text{ ns @ } C_L = 250 \text{ pF}$
- Second Source to Intel 3242  
(Detect Zero Function Not Included and Additional Chip Enable Feature Added at Pin 15)



# THE SYSTEM CLOCK

## MC6875

### M6800 TWO-PHASE CLOCK GENERATOR/DRIVER

#### M6800 CLOCK GENERATOR

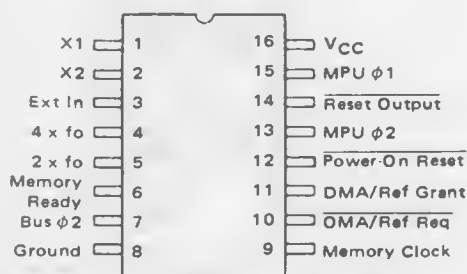
Intended to supply the non-overlapping  $\phi 1$  and  $\phi 2$  clock signals required by the microprocessor, this clock generator is compatible with 1.0, 1.5, and 2.0 MHz versions of the MC6800. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required.

#### DESCRIPTION OF PIN FUNCTIONS

- $4 \times FO$  — A free running oscillator at four times the MPU clock rate useful for a system synchro signal.
- $2 \times FO$  — A free running oscillator at two times the MPU clock rate.
- DMA/REF REQ — An asynchronous input used to freeze the MPU clocks in the  $\phi 1$  high,  $\phi 2$  low state for dynamic memory refresh or cycle steal DMA (Direct Memory Access).
- REF GRANT — A synchronous output used to synchronize the refresh or DMA operation to the MPU.
- MEMORY READY — An asynchronous input used to freeze the MPU clocks in the  $\phi 1$  low,  $\phi 2$  high state for slow memory interface.
- MPU  $\phi 1$  — Capable of driving the  $\phi 1$  and  $\phi 2$  inputs on two MC6800s.
- MPU  $\phi 2$
- BUS  $\phi 2$  — An output nominally in phase with MPU  $\phi 2$  having MC8T26A type drive capability.
- MEMORY CLOCK — An output nominally in phase with MPU  $\phi 2$  which free runs during a refresh request cycle.
- POWER-ON RESET — A Schmitt trigger input which controls Reset. A capacitor to ground is required to set the desired time constant internal 50 k resistor to  $V_{CC}$ . See General Design Suggestions for Manual Reset Operation.
- RESET — An output to the MPU and I/O devices.
- X1, X2 — Provision to attach a serie resonant crystal or RC network.
- EXT IN — Allows driving by an external TTL signal to synchronize the MPU to an external system.

#### PIN CONNECTIONS



# THE OCTAL 3-STATE BUFFER/LATCH

## MC6882A/MC3482A MC6882B/MC3482B

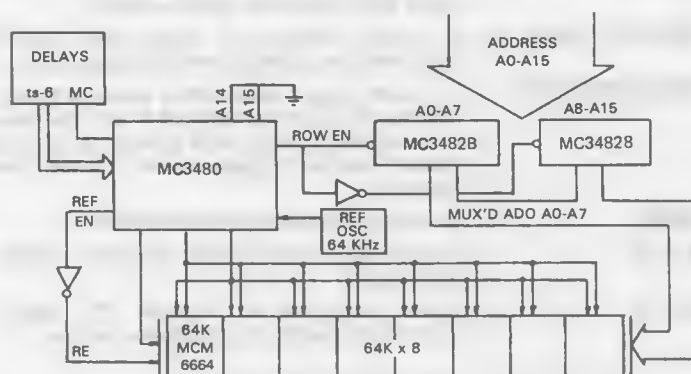
### OCTAL THREE-STATE BUFFER/LATCH

#### OCTAL THREE-STATE BUFFER/LATCH

This series of devices combines four features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows for high-speed operation; 4) 48 mA drive capability.

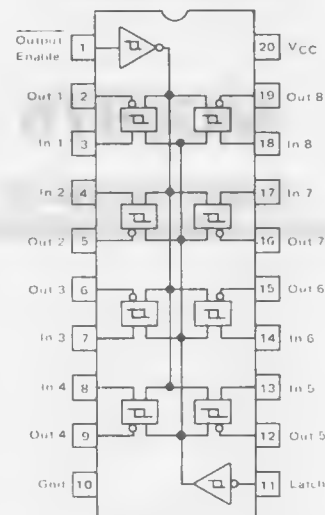
- Investing and Non Investing Options of Data
- SN74S373 Function Pinouts
- Eight Transparent Latches/Buffers in a Single Package
- Full Parallel-Access for Loading and Reloading
- Buffered Control Inputs
- All inputs Have Hysteresis to Improve Noise Rejection
- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single + 5 V Power Supply Requirement
- Compatible with 74S Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

TYPICAL 64K X 8 MEMORY SYSTEM  
USING MCM6664 RAM AND  
MC3480/MC3482B CONTROLLER/MUX.



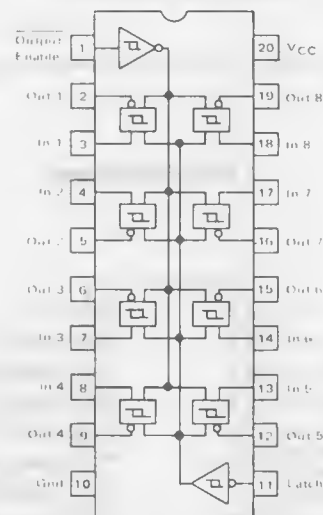
### PIN CONNECTIONS AND TRUTH TABLES

#### MC6882A/MC3482A



Output Enable	Latch	Input	Output
0	1	0	0
0	1	1	1
0	0	x	O <sub>0</sub>
1	x	x	z

#### MC6882B/MC3482B



Output Enable	Latch	Input	Output
0	1	0	0
0	1	1	1
0	0	x	O <sub>0</sub>
1	x	x	z

# THE MEMORY ERROR / CORRECTION CIRCUIT

## MC68540\*

\* To be introduced

### ERROR CHECK/CORRECT

The Error Check/Correct (ECC) device is the link between the Memory and the Central Processing Unit (CPU) that performs the task of detecting and correcting errors. The ECC will correct single bit errors and detect double errors. Control of the device allows override of correction during read and several diagnostic functions during read and write for system debug purposes.

#### Features

- Directly usable with 8-bit or 16-bit data
- Expandable for use with 32-bit data
- Bi-directional data and check bits
- Single error correction, double error detection (SEC/DED)
- Detects catastrophic error of all "1" or all "0"
- Independent byte control
- Parity bit for each byte
- Error Flags
- Several diagnostic modes
- Internal diagnostic register
- Syndromes available for hardware latching
- Input and output data latched

### OVERVIEW

This device contains the logic necessary to generate six check bits on a 16-bit data field according to a specific Hamming code. The device can also be used to generate the 5 check bits for a single 8-bit data word. Two of these devices can be used in parallel to generate the 7 check bits required for a 32-bit data field.

On reading from memory, this device will correct any single bit errors and detect any double bit errors.

In addition, various other functions are provided, which include independent byte control, error flags, and several diagnostic features.

Single error correction and double error detection (SEC/DED) are achieved by adding redundancy to the data field. The parity bits that provide this redundancy are also commonly referred to as check bits. These check bits are stored in parallel with the data bits, requiring an extra wide memory.

Upon recovery from memory, parity bits are again generated and compared with the check bits recovered, to produce the syndrome bits.

If the syndrome bits are all zero, the two parity fields agree, and no detectable error has occurred in writing and reading. If the two fields differ, an error has occurred and the configuration of the syndrome field identifies the particular bit in error. The error-correction logic then inverts this bit, so that all the data bits returned are correct. The syndrome field is also made available for error logging.

Figure 1 shows this part in a typical system.

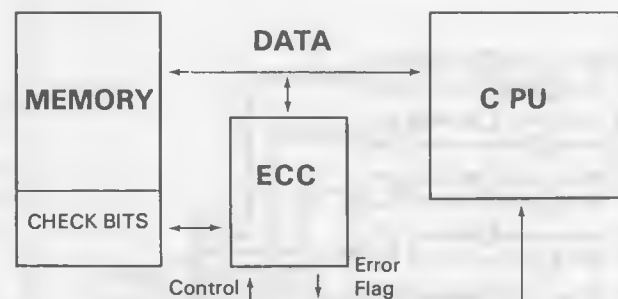


FIGURE 1 - SYSTEM BLOCK DIAGRAM

# THE EIGHT-BIT EQUAL-TO COMPARATOR

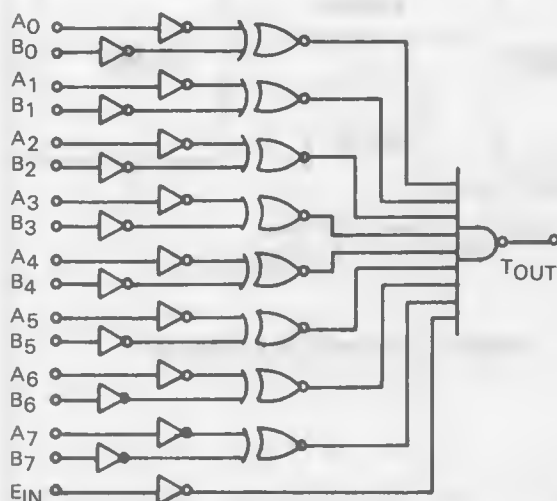
## Am25LS2521\*

\* To be introduced

### DISTINCTIVE CHARACTERISTICS

- 8-bit byte oriented equal comparator
- Cascadable using  $E_{IN}$
- High-speed, Low-Power Schottky technology
- $t_{pd} A \bullet B$  to  $E_{OUT}$  in 9ns
- Standard 20-pin package
- 100% product assurance screening to MIL-STD-883 requirements

### LOGIC DIAGRAM

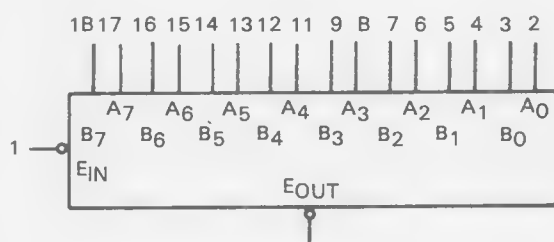


### FUNCTIONAL DESCRIPTION

The Am25LS2521 is an 8-bit "equal to" comparator capable of comparing two 8-bit words for "equal to" with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the  $E_{IN}$  produces an active LOW on the output  $E_{OUT}$ .

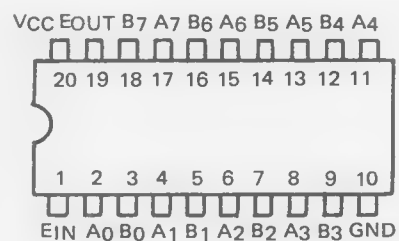
The logic expression for the device can be expressed as:  $E_{OUT} = (A_0 \odot B_0) (A_1 \odot B_1) (A_2 \odot B_2) (A_3 \odot B_3) (A_4 \odot B_4) (A_5 \odot B_5) (A_7 \odot B_7) E_{IN}$ . It is obvious that the expression is valid where  $A_0 - A_7$  and  $B_0 - B_7$  are expressed as either assertions or negations. This is also true for pair of terms i.e.  $A_0$  can be compared with  $B_0$  at the same time  $A_1$  is compared with  $B_1$ . It is only essential that the polarity of the paired terms be maintained.

### LOGIC SYMBOL



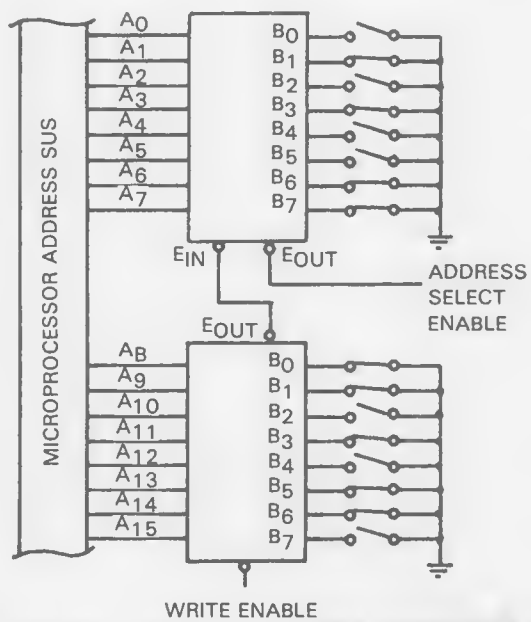
V<sub>CC</sub> = Pin 20  
GND = Pin 10

### CONNECTION DIAGRAM



Note: Pin 1 is marked for orientation

### APPLICATION



MAX. ENABLE (HIGH-to LOW) DELAY  
OVER 16-BITS  
(Commercial Range)

t <sub>PHL</sub>	A <sub>1</sub> or B <sub>1</sub> to E <sub>OUT</sub>	19ns
t <sub>PHL</sub>	E <sub>IN</sub> to E <sub>OUT</sub>	12.5ns
Total		31.5ns

MICROPROCESSOR ENABLE CONTROLLED,  
SELECTABLE, ADDRESS DECODER



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